SEC.807

What is claimed is:

1. A ball grid array package semiconductor device, the device being supplied with two or more external powers including a first power and a second power, the device comprising:

a semiconductor chip having a plurality of pads arranged along a center of a surface thereof;

a substrate having a slot of a predetermined size and centrally arranged in a spaced relationship to the plurality of pads, the substrate having a signal line plane including a signal line pattern and a plurality of ball mounts on its one side, and wherein the semiconductor chip is mounted on an other side thereof;

a bonding material inserted between the semiconductor chip and the substrate to fix the semiconductor chip to the substrate; and

a plurality of balls mounted on the plurality of ball mounts to be connected to an external circuit,

wherein the signal line plane is divided into two or more signal line planes including a first line plane and a second line plane, and

wherein lines for the first power are formed only on the first signal line plane, and lines for the second power are formed only on the second signal line plane.

2. The ball grid array package semiconductor device of claim 1, wherein the lines for the first power are combined with each other on the first signal line plane, thereby forming a first combined plane exhibiting a single node

electrically, and the lines for the second power are combined with each other on the second signal line plane, thereby forming second combined plane exhibiting a single node electrically.

3. The ball grid array package semiconductor device of claim 1, wherein the device is a chip scale package semiconductor device.

4. The ball grid array package semiconductor device of claim 1, wherein the first power has a positive voltage and the second power is ground.

5. The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to the P-substrate and a pocket P-well of the semiconductor chip.

6. The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to one of the P-substrate and a pocket P-well of the semiconductor chip.

7. The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a twin-well structure, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to a P-substrate of the semiconductor chip.

8. A ball grid array package semiconductor device, the device being supplied with two or more external powers, the device comprising:

a semiconductor chip having a pad at its center of a surface thereof;

a substrate having a slot of a predetermined size and centrally arranged in a spaced relationship to the pad, the substrate having a signal line plane including a signal line pattern and a plurality of ball mounts on its one side, and wherein the semiconductor chip is mounted on an other side thereof;

a bonding material inserted between the semiconductor chip and the substrate to fix the semiconductor chip to the substrate; and

a plurality of balls mounted on the plurality of ball mounts to be connected to an external circuit,

wherein the signal line plane is divided into a plurality of signal line planes, and lines for at least one selected power among the external powers are formed only on a corresponding signal line plane.

9. The ball grid array package semiconductor device of claim 8, wherein the lines for the at least one selected power among the external powers are combined with each other on the corresponding signal line plane, thereby

forming a combined plane exhibiting a single node electrically.

10. The ball grid array package semiconductor device of claim 8, wherein the device is a chip scale package semiconductor device.

11. A ball grid array package semiconductor device having a plurality of balls, including a plurality of power balls and a plurality of ground balls, the ball grid array package semiconductor device comprising:

a semiconductor chip comprising a plurality of pads, including a plurality of power pads and a plurality of ground pads, arranged along a center of a surface thereof; and

a single layer substrate including a slot of a predetermined size centrally arranged in a spaced relationship to the plurality of pads, and, on one side thereof having

a power plane on a first portion of a surface of the one side around the slot, the power plane including power ball mounts, power balls and the power pads;

a ground plane on a second portion of the surface of the one side around the slot, the ground plane including ground ball mounts, ground balls and the ground pads; and

a plurality of signal ball mounts,

wherein the semiconductor chip is mounted on an other side of the substrate such that the plurality of pads are electrically connected to the power

ball mounts, the ground ball mounts and the signal ball mounts.

12. The ball grid array package semiconductor device of claim 11, wherein a boundary defining the power plane wraps around signal ball mounts positioned on the power plane and their interconnection lines.

13. The ball grid array package semiconductor device of claim 11, wherein a boundary defining the ground plane wraps around signal ball mounts positioned on the ground plane and their interconnection lines.

14. The ball grid array package semiconductor device of claim 11, further comprising a power ball mount separated from the power plane and connected to an external circuit.

15. The ball grid array package semiconductor device of claim 11, further comprising a ground ball mount separated from the ground plane and connected to an external circuit.